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EXAMINER	
NGUYEN, QUANG N	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,020	HARRIS, GORDON J.	
	Examiner	Art Unit	
	Quang N. Nguyen	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-20 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-20 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is in responsive to the Amendment filed on 02/03/2006. Claim 6 has been amended. Claims 12-13 and 21-22 have been canceled. Claims 23-25 have been added as new claims. Claims 1-11, 14-20 and 23-25 remain for examination.

Claim Objections

2. Claim 1, 14, 24 and 25 are objected to because of the following informalities:

On line 8 of claim 1: "the logical page is associated with said the plurality of physical memory clusters" should be "the logical page is associated with [[~~said~~]] the plurality of physical memory clusters.

On line 1 of claim 14: "An article comprising a computer-readable medium" should be "An article comprising a computer-readable storage medium".

On line 1 of claim 24: "The method of claim 6" should be "The system of claim 6".

On line 1 of claim 25: "The method of claim 14" should be "The article of claim 14".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nijhawan et al. (US 6,374,341), hereinafter "Nijhawan", in view of Vishin et al. (US 5,860,146), hereinafter "Vishin", and further in view of Applicant Admitted Prior Art (AAPA).

5. As to claim 1, Nijhawan teaches a method comprising:

moving data into a physical memory page, and the physical memory page comprising a plurality of physical memory clusters *(moving data into a plurality of memory blocks 92 and 94 that are aligned as illustrated in Fig. 9)* (Nijhawan, Fig. 9);

creating a logical page providing an aligned view of the data *(a logical page is created/mapped to a physical page)* (Nijhawan, Fig. 9 and C3:L60 – C4:L27);

establishing a relationship between the logical page and the physical memory page such that the logical page is associated with the plurality of physical memory clusters *(a logical page number is mapped or translated to a physical page number, and the target physical location within the page can be accessed, as illustrated in Fig. 9)* (Nijhawan, Fig. 9 and C4: L3-27);

forwarding a list of the logical pages to a storage resource such that the data referenced by the logical pages are stored subsequently into a storage resource *(as in Fig. 8, the linear address translation maintains all memory blocks are aligned, no two such memory blocks are mapped in the same linear address, hence no overlapping mappings, i.e., stored subsequently, and the block of memory is correctly sized-aligned in physical memory as illustrated in Fig. 9)* (Nijhawan, C9: L26-37 and C10: L7-16).

However, Nijhawan does not explicitly teach moving data from a network layer into a physical memory page, wherein the network layer receives and transmits the data as data packets that are odd sized, arrive asynchronously, and contain metadata embedded with real data.

In an analogous art, Vishin teaches a distributed computer system having a primary translation lookaside buffer for storing page table entries and translating virtual *(logical)* addresses into physical addresses governed by a memory controller 112 that can also send requests via a network 114 to pull in pages of data stored in the memory stores or secondary memory of other clusters 102 or other devices coupled to the network 114 *(in order to moving/accessing/writing data from/to a remote cluster 102 via the network 114 to pull in pages of data stored in the memory stores or secondary memory of other clusters 102 as illustrated in Fig. 1, one of ordinary skill in the art would be appreciated that it should include the step of moving data from a network layer into the memory stores, i.e., into a physical memory space)* (Vishin, Fig. 1 and C1: L12-24).

Also, Applicant Admitted Prior Art (AAPA) teaches in an Ethernet network, network data can be transmitted and received as data packets that can be

characterized as being odd-sized, arriving asynchronously or without warning, and having metadata such as protocol information embedded along with real data (AAPA, Background, page 1, lines 8-12).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Nijhawan, Vishin and AAPA to include moving data from a network layer into a physical memory page, wherein the network layer receives and transmits the data as data packets that are odd sized, arrive asynchronously, and contain metadata embedded with real data since such methods were conventionally employed in the art to extend the address space to memory outside the cluster by using virtual memory management subsystem to manage access to remote physical address through the use of a (remote) page table and/or an auxiliary translation lookaside buffer (TLB) (Vishin, C1: L5-9 and L54-63).

6. As to claim 2, Nijhawan-Vishin-AAPA teaches the method of claim 1, further comprising: dividing the physical memory pages into physical memory clusters *(dividing the memory into memory block size from 4K to 4M)* such that the data received by the network layer is stored into the physical memory clusters *(i.e., data is stored in memory blocks 92 and 94 as illustrated in Fig. 9)* (Nijhawan, Fig. 9 and C10: L7-16).

7. As to claim 3, Nijhawan-Vishin-AAPA teaches the method of claim 1, further comprising: creating a plurality of logical pages based on the offset and length of the data associated with a network drive operation (Nijhawan, C7: L3-18 and C8: L40-51).

8. As to claim 4, Nijhawan-Vishin-AAPA teaches the method of claim 1, further comprising: creating a read only logical page comprising zeros, i.e., comprising un-initialized data *(the OS ensures that all memory blocks are aligned on a 4M linear address boundary so that the lower 22 bits of the starting linear address of the memory blocks are zero)* (Nijhawan, C2: L1-5).

9. As to claim 5, Nijhawan-Vishin-AAPA teaches the method of claim 1, further comprising: merging an existing physical memory cluster with a new physical cluster based on the offset and length of the existing physical memory cluster and based on the offset and length of the new physical memory cluster *(within the allocated 128K of memory, the OS inherently maps 64K block of memory that resides in physical memory on 64K boundaries, which can be used for the desired 40K block, and then the extra memory on either side of the 64K boundaries can be reallocated/remerged)* (Nijhawan, C9:L61 – C10:L7).

10. Claims 6-11 are corresponding system claims of method claims 1-5; therefore, they are rejected under the same rationale.

11. Claims 14-18 are corresponding computer-readable medium claims of method claims 1-5; therefore, they are rejected under the same rationale.

12. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nijhawan-Vishin-AAPA, and further in view of Richter (US 2003/0097481 A1).

13. As to claims 19-20, Nijhawan-Vishin-AAPA teaches the method of claim 1, but does not explicitly teach the network layer uses a transport control protocol / internet protocol (TCP/IP) to transmit and receive the data as data packets over a computer network such as an Ethernet.

In an analogous art, Richter teaches a content delivery system that receives and transmits data packets, wherein the network interface engine *(i.e., the network layer)* performs the MAC, IP, TCP or UDP header identification, verification and checksum validation/generation, etc., in receiving and transmitting the data packets (Richter, paragraph [0072]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Nijhawan-Vishin-AAPA and Richter to use TCP/IP to transmit and receive the data as data packets over the Ethernet network since such methods were conventionally employed in the art to allow the system using the well-established networking protocol stack TCP-UDP/IP suite to verify end-to-end data integrity to ensure that intermediate forwarding notes, client memory problems, and statistically remote errors have not corrupted the original data packets outside of media layer detection in transmitting and receiving the data packets over the Ethernet network (Richter, paragraph [0003]).

14. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nijhawan-Vishin-AAPA, and further in view of Westbrook et al. (US 6,934,760), hereinafter "Westbrook".

15. As to claim 23, Nijhawan-Vishin-AAPA teaches the method of claim 1, but does not explicitly teach the data packets arrive in a sequence that is different from an original sequence in which they were transmitted.

In an analogous art, Westbrook teaches typically, packets of the original stream are marked with a sequence number, timestamp, or other ordering indication, and then dynamically routed and distributed among different paths and arriving at a location possibly out of their original sequence *(data packets arrive in a sequence that is different from an original sequence in which they were transmitted)* (Westbrook, Abstract and C3: L40-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Nijhawan-Vishin-AAPA and Westbrook to include the data packets arrive in a sequence that is different from an original sequence in which they were transmitted because it is typically more cost-effective and technically feasible to provide multiple slower rate links or switching paths, than to provide a single higher rate path and such designs also achieve other desired performance characteristics (Westbrook, C1: L28-36).

16. Claims 24-25 are corresponding system and article claims of method claim 23; therefore, they are rejected under the same rationale.

Response to Arguments

17. In the remarks, Applicant argued in substance that

(**A**) Neither Nijhawan, Vishin, nor AAPA provide any suggestion as to why one skilled in the art would be motivated to modify Nijhawan's method with the teaching of Vishin and AAPA in the manner suggested by the Examiner.

As to point (**A**), in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, **Nijhawan** teaches an invention for variable size paging using fixed size TLB (Translation Lookaside Buffer) entries; in particular, a paging system translates a linear (or virtual/logical) address into a physical address by mapping/translating a logical page number into a physical page number and then the

target physical location within the page can be accessed **(Nijhawan, Abstract and C3: L44-52 and C4: L3-27)**. In an analogous art, **Vishin** also teaches a computer system includes a data processor, a primary translation lookaside buffer (TLB) for storing page table entries and translating virtual/logical addresses into physical addresses by a memory controller 112 that can also sends requests via a network 114 to pull in pages of data stored in the memory stores or secondary memory of remote data clusters 102 or other devices coupled to the network 114 **(Vishin, Abstract and C1: 12-24)**. And also, **Applicant Admitted Prior Art (AAPA)** teaches in an Ethernet network, network data can be transmitted and received as data packets that can be characterized as being odd-sized, arriving asynchronously or without warning, and having metadata such as protocol information embedded along with real data **(AAPA, Background, page 1, lines 8-12)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of **Nijhawan**, **Vishin** and **AAPA** to include moving data from a network layer into a physical memory page, wherein the network layer receives and transmits the data as data packets that are odd sized, arrive asynchronously, and contain metadata embedded with real data since such methods were conventionally employed in the art to extend the address space to memory outside the local data memory/cluster by using virtual memory management subsystem to manage access to remote physical address/memory of other remote data clusters over the network, through the use of a (remote) page table and/or an auxiliary translation lookaside buffer (TLB) **(Vishin, C1: L5-9 and L54-63)**.

(**B**) Nijhawan lacks disclosure of a network altogether and Vishin neither discloses nor suggests that the network 114 is capable of transmitting and receiving data as data packets.

As to point (**B**), in response to applicant's arguments against the references individually (such that "Nijhawan lacks disclosure of a network altogether"), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, **Vishin** teaches a distributed computer system having a primary translation lookaside buffer for storing page table entries and translating virtual *(logical)* addresses into physical addresses governed by a memory controller 112 that can also send requests via a network 114 to pull in pages of data stored in the memory stores or secondary memory of other clusters 102 or other devices coupled to the network 114 *(Examiner respectfully submits that one of ordinary skill in the art would be appreciated that in order to moving/accessing/writing data from/to a remote cluster 102 via the network 114 to pull in pages of data stored in the memory stores or secondary memory of other clusters 102 as illustrated in Fig. 1, it should include the step of transmitting and receiving data as data packets before storing data into the memory stores, i.e., storing data into a physical memory space)* **(Vishin, Fig. 1 and C1: L12-24).**

18. Applicant's arguments as well as request for reconsideration filed on 02/03/2006 have been fully considered but they are not deemed to be persuasive.

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Further references of interest are cited on Form PTO-892, which is an attachment to this office action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Nguyen whose telephone number is (571) 272-3886.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's SPE, Rupal Dharia, can be reached at (571) 272-3880. The fax phone number for the organization is (571) 273-8300.

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RUPAL DHARIA
SUPERVISORY PATENT EXAMINER